1.(Previously Presented): A method for controlling the operation of a SAR conversion cycle, comprising the steps of:

initiating the SAR conversion cycle by connecting one side of a plurality of capacitors in a capacitor array to a first capacitor reference voltage in the other side of the plurality of capacitors to the input of a comparator;

sequentially switching in a plurality of compare cycles the one side of a select one or ones of the capacitors to a second capacitor reference voltage to change the voltage on the input of the comparator;

initiating a compare operation after initiation of each compare cycle to compare the value on the input of the comparator with a compare reference voltage after a predetermined settling time has elapsed from the beginning of the initiation of each compare cycle; and

during the compare cycle, reducing transients due to voltage variations on the input of the comparator as a result of the step of sequentially switching, the reduction operating for a predetermined portion of the associated compare cycle.

2. (Currently Amended): The method of Claim 1, wherein the comparator has a variable gain [[in]] and the step of reducing transients comprises reducing the gain of the comparator for the predetermined portion of the compare cycle.

3.(Previously Presented): The method of Claim 2, wherein the predetermined portion of the compare cycle comprises a portion of the initiation of the associated compare cycle which begins when the one side of the associated select one or ones of the capacitors in the capacitor array is connected to the second comparator reference voltage.

4.(Previously Presented): The method of Claim 3, wherein the duration of the predetermined portion is less than the length of the compare cycle.

5.(Currently Amended): The method of Claim 2, wherein the comparator is comprised of a plurality of stages, and the step of reducing the gain of the comparator comprises the step of terminating the output of selected ones of the stages with a predetermined termination to reduce the signal input to the next successive stage.

6.(Currently Amended): The method of Claim 2, wherein the step of reducing the gain of the comparator comprises generating a blocking pulse when the select one or ones of the plurality of capacitors in the capacitor ~~arrays~~ array are switched in the step of sequentially switching for a given compare cycle, which blocking pulse has a predetermined length during which the gain of the comparator is reproduced.

7. (Previously Presented): The method of Claim 6, wherein the step of generating a blocking pulse comprises generating blocking pulses of different durations for at least two of the compare cycles.

8. (Previously Presented): The method of Claim 6, wherein the length of the compare cycle is different for at least one of the compare cycles in the SAR conversion cycle.